AMENDMENTS TO THE CLAIMS:

Please amend the Claims as follows:

1 – 15. (Cancelled)

16. (Currently Amended) A common memory controller capable of controlling different types of memory chips which are connected to a common bus, comprising:

a first interface portion for receiving a control output signal to access said memory ~~chip~~ chips from a controller, and outputting a control input signal to the controller;

a conversion control portion for converting said control output signal into a memory input signal in response to a specification of [[a]] each of said memory ~~chip~~ chips to which the memory controller is connected, and converting a memory output signal output from the memory ~~chip~~ chips into the control input signal receivable to said controller;

a second interface portion for outputting the memory input signal and receiving the memory output signal; and

a plurality of terminals coupled to the second interface portion~~, and capable of connecting at least one of the different types of memory chips~~ for connecting the second interface portion to the different types of memory chips via said common bus.

17. (Previously Presented) The common memory controller according to claim 16, wherein the different types of memory chips include a synchronous DRAM or a synchronous SRAM.

18. (Previously Presented) The common memory controller according to claim 16, further comprising

a memory unit for storing the specification of the memory chip, and wherein the memory unit is programmable.

19. (Previously Presented) The common memory controller according to claim 16, wherein the specification of memory chip includes a memory type, a command sequence, an address sequence or latency information.

20. (Currently Amended) The common memory controller according to claim 16, wherein the second interface ~~unit~~ portion controls an output timing of the memory input signal in response to the specification of memory chip.

21. (Previously Presented) The common memory controller according to claim 16, wherein the memory input signal includes an address, a command, and data.

22. (Previously Presented) The common memory controller according to claim 21, wherein the memory input signal further includes a chip select signal.

23. (Previously Presented) The common memory controller according to claim 21, wherein the memory input signal further includes a direct memory access control signal.

24. (Previously Presented) The common memory controller according to claim 16, wherein the number of the plurality of terminals is larger than that of the terminals of each of the memory chips to which the memory controller is connected.

25. (Previously Presented) The common memory controller according to claim 16, wherein the plurality of terminals include control terminals, address terminals, data terminals, and a clock terminal.

26. (Currently Amended) A multi chip package comprising:

a system LSI chip including a common memory controller capable of controlling different types of memory chips which are connected to a common bus; and

[[a]] memory ~~chip~~ chips coupled to the system LSI chip, and controlled by the common memory controller,

the common memory ~~chip~~ controller including:

a first interface portion for receiving a control output signal to access said memory ~~chip~~ chips from a controller of the LSI chip, and outputting a control input signal to the controller;

a conversion control portion for converting said control output signal into a memory input signal in response to a specification of each of the memory ~~chip~~ chips, and converting a memory output signal from the memory ~~chip~~ chips into the control input signal receivable to said controller;

a second interface portion for outputting the memory input signal and receiving the memory output signal; and

a plurality of terminals coupled to the second interface portion, for connecting the second interface portion to the different types of memory ~~chip~~ chips via said common bus.

27. (New) The common memory controller according to claim 16, further comprising

an arbiter circuit for arbitrating an order to access said memory chips when access requests for said memory chips overlap with each other.